Attorney Docket No. NVID-062/00US
Client Reference No. P000731

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Michael M. Klock	Confirmation No.:	5104
Serial No.:	10/694,923	Group Art Unit:	2628
Filed:	October 27, 2003	Examiner:	WASHBURN, Daniel C.

For: **METHOD, APPARATUS AND SYSTEM FOR ADAPTIVE PERFORMANCE LEVEL MANAGEMENT OF A GRAPHICS SYSTEM**

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In response to the Final Office Action mailed October 9, 2007, please amend the above-identified patent application in the following manner.

Amendments to the Claims are reflected in the listing of claims that begins on page **2** of this paper.

Remarks begin on page **5** of this paper.

IN THE CLAIMS:

Set forth below in ascending order, with status identifiers, is a complete listing of all claims currently under examination. Changes to any amended claims are indicated by strikethrough and underlining. This listing also reflects any cancellation and/or addition of claims.

1. (previously presented) A method of operating a graphics system having a sequence of at least two discrete performance levels with each performance level being defined by a core clock rate of a graphics processing unit and a memory clock rate, the method comprising:

monitoring a first attribute indicative of utilization of a graphics pipeline within a graphics processor core clock domain and determining whether the graphic pipeline is under-utilized or over-utilized;

monitoring a second attribute indicative of utilization of a graphics memory within a graphics memory clock domain and determining whether the graphics memory is under-utilized or over-utilized;

selecting a performance level display rate within a normal range by increasing the performance level in response to detecting an over-utilization condition and decreasing the performance level in response to detecting an under-utilization condition; and

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal range.

2-6. (cancelled)

7. (previously presented) The method of claim 1, wherein monitoring said first attribute comprises:

monitoring the percentage of clock cycles in a graphics pipeline for which at least one stage is held up waiting for the results of another stage.

8. (previously presented) The method of claim 1, wherein said monitoring said second attribute comprises: monitoring the percentage of clock cycles in a graphics memory for which a memory bandwidth of said graphics memory is inadequate.

9-20. (cancelled)

21. (previously presented) A method of operating a graphics system having a sequence of at least two discrete performance levels where each performance level is defined by a core clock rate of a graphics processing unit and a memory clock rate, the performance levels including a high performance level for processing complex three-dimensional graphical images and at least one lower power, lower performance level for processing less complex graphical images, the method comprising:

monitoring as a function of time attributes of a graphics pipeline and a graphics memory of said graphics system that are indicative of a level of utilization of said graphics system;

in response to detecting a level of utilization greater than an over-utilization threshold for which a display rate of the graphics system is likely to be significantly decreased below a normal display rate, selecting a higher performance level;

in response to detecting a level of utilization below an under-utilization threshold, selecting a lower performance level to reduce power required by the graphics system; and

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal range.

22-24. (cancelled)

25. (currently amended) A graphics system, comprising:

a graphics processor having a sequence of at least two discrete performance levels where each performance level is defined by a graphics processor core clock rate of a graphics processing unit and a memory clock rate~~, the performance levels including~~;

a graphics memory coupled to said graphics processor by a graphics bus and operable at said memory clock rate;

a performance level controller, said performance level controller configured to monitor, as function of time, at least one attribute of said graphics system indicative of a level of

utilization of at least one component of said graphics system for which over-utilization of said component decreases a display rate, and

said performance level controller configured to increase said performance level to avoid over-utilization of said at least component;

said performance level controller configured to decrease said performance level from a high performance level to a lower performance level to avoid under-utilization of said at least one component;

the graphics system operating at the core clock rate and memory clock rate associated with the performance level selected by the performance level controller, the selected performance level being a minimum performance level capable of maintaining the display rate within a normal range.

26-27. (cancelled)

28. (new) The method of claim 1, wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

29. (new) The method of claim 21, wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

30. (new) The graphics system of claim 25, wherein the performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

REMARKS

This communication is in response to the Final Office Action of October 9, 2007.

The Examiner objected to claim 25. Applicant has made the requested correction.

New claims 28-30 were added which specify that there are at least four performance levels, including "a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level." Support for this claim amendment is found in paragraph [0024].

Applicants respectfully traverse the 35 USC §§ 102-103 claim rejections. Regarding independent claims 1, 21, and 25, one of ordinary skill in the art would not combine Giemborek and Williams to achieve Applicant's claimed invention. Giemborek does not measure processor utilization. In contrast, Giemborek reads display mode settings to make processor clock adjustments, with the display mode settings being described in column 6, line 66 to column 7, line 4 as "color depth, screen resolution, screen size, refresh rate, or the number of active CRT controllers driving displays attached to the device." Williams does not have discrete performance settings, but instead always attempts to operate the processor as fast as possible for the heat load, as described in column 6, lines 26-32. Consequently, the references fail to teach a number of limitations and in addition one of ordinary skill in the art would not combine their teachings.

It is also further respectfully submitted that the cited art does not teach or suggest discrete performance levels further in which "the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal range." As previously described, Williams always attempts to operate as fast as possible. Giemborek does not discuss maintaining a display rate within a normal range.

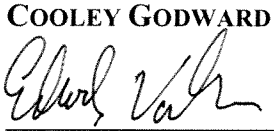
Regarding new claims 28-30, the cited art further does not teach or such four different discrete performance levels including "a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level."

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 50-1283.

Respectfully submitted,
COOLEY GODWARD KRONISH LLP

Dated: October 24, 2007

By: 

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